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CLAIMS 1 – 5 (CANCELLED)

Claim 6 (New): A latch circuit, comprising:

a first latch portion including a first clock transistor; and

a second latch portion including a second clock transistor;

wherein the first and second clock transistors form a transistor clock pair and the first clock transistor has a different property or characteristic to the second clock transistor such that a ratio of a hold period to a follow period of the transistor clock pair is greater than 1.

Claim 7 (New): The latch circuit according to claim 6, wherein the different property or characteristic comprises a difference in emitter area.

Claim 8 (New): The latch circuit according to claim 7, wherein the emitter area of the first clock transistor is greater than that of the second clock transistor.

Claim 9 (New): The latch circuit according to claim 8, wherein the emitter area of the first clock transistor is double that of the second clock transistor.

Claim 10 (New): A prescaler circuit including a first and second latch circuit according to claim 6.

Claim 11 (New): A prescaler circuit including a first and second latch circuit according to claim 7.

Claim 12 (New): A prescaler circuit including a first and second latch circuit according to claim 8.

Claim 13 (New): A prescaler circuit including a first and second latch circuit according to claim 9.